



TS #	1				28				56				84			
	1234	1234	1234	1234	1234	1234	1234	1234	1234	1234	1234	1234	1234	1234	1234	
STS1 slot #	1	1234	1234	1234	1234	1234	1234	1234	1234	1234	1234	1234	1234	1234	1234	
	T or				T or							T or				
	1 E				1 E							1 E				
	# 1				# 1							# 1				
	1 #				2 #							3 #				
	1				2							3				

[illegible][illegible][illegible]

Fig. 2

The diagram illustrates a multi-processor system with four components: Sender-1, Sender-2, Receiver-1, and Receiver-2. Each component has a set of 8-bit data and control signals (RxData7-0, RxValid, RxFrm\_ind, RxFrm\_pos2-0, RxPrty, TxData7-0, TxValid, TxFrm\_ind, TxFrm\_pos2-0, TxPrty2, TxPrty1) and IFSlot control signals (RxlFSlot\_IO, TxIFSLOT\_IO, Clk\_in). Sender-1 and Sender-2 are connected to Receiver-1 and Receiver-2 via a common bus. A clock source is connected to the Clk\_in of all components. Handwritten labels 116, 117, 118, and 119 are present near the components.

FIG. 3